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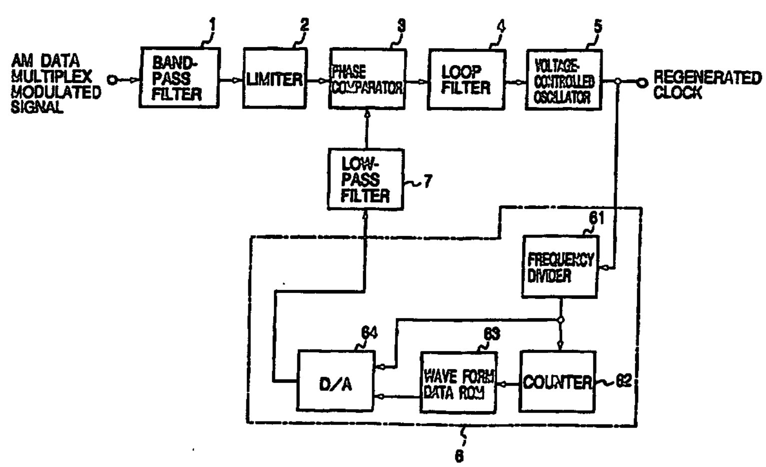
(54) CLOCK REGENERATION CIRCUIT

(57) A clock regeneration circuit for regenerating a clock signal for demodulating data from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of an amplitude-modulated signal at the same time. The carrier for an amplitude-modulated signal is extracted from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of the amplitude-modulated signal at the same time through a band-pass filter (1), and the oscillation frequency of a voltage-controlled oscillator (5) is controlled by the output of a phase comparator (3) through a loop filter (4). The oscillation output of the voltage-controlled oscillator (5) is supplied to a direct digital synthesizer (6) and the phase of the carrier extracted through the band-pass filter (1) is compared with the phase of the output of the direct digital synthesizer (6) by means of the phase comparator (3). The oscillation output of the voltage-controlled oscillator (5) is then synchronized with the carrier for the amplitude-modulated signal to produce a clock signal for demodulating data.

FIG. 1



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sizer for inputting the oscillation output from the voltage-controlled oscillator and supplying an output to the frequency-converting means as a local oscillation output, wherein the oscillation output of the voltage-controlled oscillator is used as a clock signal for data demodulation from the AM data multiplex modulated signal.

[0010] According to this clock regeneration circuit of this invention, the carrier extracting means extracts the carrier of the AM modulated signal from the frequency-converted AM data multiplex modulated signal, the phases of the extracted carrier and an output of the first direct digital synthesizer are compared by the phase comparator, and in accordance with a phase comparison result, the oscillation frequency of the voltage-controlled oscillator is controlled. The oscillation output of the voltage-controlled oscillator is supplied to the frequency-converting means as a local oscillation output. Accordingly, the oscillation output of the voltage-controlled oscillator is synchronized with the carrier of the AM modulated signal, and the oscillation output of the voltage-controlled oscillator can be used as the clock signal for demodulating the digital modulated signal separated from the AM data multiplex modulated signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Fig. 1 is a block diagram showing the structure of a clock regeneration circuit according to an embodiment of the invention, Fig. 2 is a block diagram showing the structure of an AM data multiplex modulated signal generating apparatus used for explaining the clock regeneration circuit of the embodiment, Fig. 3 is a schematic diagram illustrating the operation of the AM data multiplex modulated signal generating apparatus shown in Fig. 2, and Fig. 4 is a block diagram showing the structure of a clock regeneration circuit according to another embodiment of the invention.

EMBODIMENTS OF THE INVENTION

FIRST EMBODIMENT

[0012] A clock regeneration circuit of this invention will be described with reference to preferred embodiments. Fig. 1 is a block diagram showing the structure of a clock regeneration circuit according to a first embodiment of the invention.

[0013] Prior to describing the clock regeneration circuit of the invention, an apparatus for generating an AM data multiplex modulated signal will be described with reference to Fig. 2.

[0014] In the AM data multiplex modulated signal generating apparatus, an analog signal (hereinafter simply called an input signal where applicable), such as a voice signal or the like is supplied to an AM modulator 11 in which the input signal is AM-modulated by a carrier having a frequency of fc generated by a frequency divider 112 to be later described. The AM modulator 11 is composed of an A/D converter 111 for A/D converting the input signal and a multiplier 112 for AM-modulating an output of the A/D converter 111.

[0015] The AM data multiplex modulated signal generating apparatus also includes a QPSK baseband signal generator 12 which is composed of: a master clock oscillator 121 for oscillating at a frequency of, e.g., 32 MHz; a frequency divider 122 for dividing an oscillation frequency of the master clock oscillator 121 to generate signals having frequencies of 2 MHz and 6 kHz; a direct digital synthesizer 123 for receiving a signal having a frequency of 2 MHz from the frequency divider 122 and generating the carrier having the frequency of fc, two orthogonal signals having a frequency of $(fc + f\alpha)$ and two orthogonal signals having a frequency of $(fc - f\alpha)$; and a serial/parallel converter 124 for converting serial digital data I and Q of 6 kbps into parallel digital data I and Q. The QPSK baseband digital signal generator 12 outputs QPSK baseband digital signals from the serial/parallel converter 124. An output signal having a frequency of 2 MHz is used as a clock signal for the A/D converter 111, an output signal having a frequency fc is supplied as a clock signal of the AM modulator 112, and an output signal having a frequency of 6 kHz is supplied as a conversion clock signal of the serial/parallel converter 124.

[0016] The QPSK baseband digital signals I and Q output from the QPSK baseband digital signal generator 12 are supplied to a quadrature modulator 13 composed of multipliers 131 and 132 and an adder 133. The multiplier 131 multiplies the I data by $\cos(\omega c + \omega\alpha)t$, the multiplier 132 multiplies the Q data by $\sin(\omega c + \omega\alpha)t$, and the adder 133 adds the outputs of the multipliers 131 and 132 to thereby quadrature-modulate the carrier having a frequency of $(fc + f\alpha)$ by the QPSK baseband digital signals. The frequencies $(fc + f\alpha)$ and $(fc - f\alpha)$ correspond to the frequencies of upper and lower AM modulated side bands.

[0017] The QPSK baseband digital signals I and Q output from the QPSK baseband digital signal generator 12 are also supplied to a complex conjugator 14 which generates a complex conjugate of sign inverted digital signals I and Q. The complex conjugator 14 may be composed of an inverter 141 for inverting the I signal.

[0018] The QPSK baseband digital signals I and Q output from the complex conjugator 14 are supplied to a quadrature modulator 16 composed of multiplies 161 and 162 and an adder 163. The multiplier 161 multiplies the I data by $\cos(\omega c - \omega\alpha)t$, the multiplier 162 multiplies the Q data by $\sin(\omega c - \omega\alpha)t$, and the adder 163 adds the outputs of the multipliers 161 and 162 to thereby quadrature-modulate the carrier having a frequency of $(fc - f\alpha)$ by the QPSK baseband digital signals I and Q output from the complex conjugator 14. Output signals from the quadrature modulators 13

and 16 are added by an adder 17. An output signal from the adder 17, i.e., a digital modulated signal and an AM modulated signal output from the AM modulator are added by an adder 18. An addition signal from the adder 18 is supplied to a D/A converter 20 to convert it into an analog signal which is output as an AM data multiplex modulated signal.

[0019] An AM data multiplex modulation process by the AM data multiplex modulated signal generating apparatus shown in Fig. 2 and structured as above is schematically illustrated in Fig. 3. Referring to Fig. 3, an AM modulated signal output from the AM modulator 1 is indicated at a in Fig. 3. An output signal of the quadrature modulator 16, i.e., a digital modulated signal, is indicated at b in Fig. 3, and an output signal of the quadrature modulator 13, i.e., a digital modulated signal, is indicated at c in Fig. 3. A digital modulated signal output from the adder 17 is a sum of b and c shown in Fig. 3, and the AM data multiplex modulated signal output from the adder 18 is indicated at d in Fig. 3.

[0020] An AM data multiplex modulation process by the AM data multiplex modulated signal generating apparatus shown in Fig. 2 will be described.

[0021] An AM modulated signal vAM(t) is expressed by the following equation (1):

$$vAM(t) = \{I + \kappa vm(t)\} \cos \omega ct \tag{1}$$

where I is an amplitude of the carrier, ωc (rad/s) is an angular frequency of the carrier, κ is a modulation factor, and vm(t) is an input signal.

[0022] The I and Q signal trains generated by the QPSK baseband digital signal generator 12 are represented by In and Qn which are also called dibits, where

$$In = \pm 1$$

$$Qn = \pm 1.$$

[0023] The output signals from the QPSK baseband digital signal generator 12 are branched, one being supplied to the quadrature modulator 13 to which the carrier having the frequency (fc + fα) is supplied, whereat the carrier having an angular velocity of (ωc + ωα) (rad/s) is quadrature-modulated by the complex signal train. An output signal vDH(t) of the quadrature modulator 13 is expressed by the following equation (2):

$$vDH(t) = In \cos (\omega c + \omega \alpha)t + Qn \sin (\omega c + \omega \alpha)t \qquad (2).$$

[0024] The other output signal from the QPSK baseband digital signal generator 12 is supplied to the quadrature modulator 14 in which the signs of the output signals In and Qn are converted into (-In) and (Qn). This complex signal train is supplied to the quadrature modulator 16 to which the carrier having the frequency (fc - fα) is supplied, whereat the carrier having an angular velocity of (ωc - ωα) (rad/s) is quadrature-modulated by the complex signal train. An output signal vDL(t) of the quadrature modulator 16 is expressed by the following equation (3):

$$vDL(t) = - In \cos (\omega c - \omega \alpha)t + Qn \sin (\omega c - \omega \alpha)t \qquad (3).$$

[0025] The output signals vDH(t) and vDL(t) given by the equations (2) and (3) are added by the adder 17, and the addition signal or digital modulated signal vD(t) is given by the following equation (4):

$$\begin{aligned} vD(t) &= vDH(t) + vDL(t) \\ &= In \cos (\omega c + \omega \alpha)t + Qn \sin (\omega c + \omega \alpha)t - In \cos (\omega c - \omega \alpha)t + Qn \sin (\omega c - \omega \alpha)t \end{aligned} \qquad (4).$$

[0026] The AM modulated signal vAM(t) and digital modulated signal vD(t) are added by the adder 18, and the AM data multiplex modulated signal v(t) is expressed by the following equation (5) by using the equations (1) and (4):

$$\begin{aligned} v(t) &= vAM(t) + vD(t) \\ &= \{I + \kappa vm(t)\} \cos \omega ct + In \cos (\omega c + \omega \alpha)t + Qn \sin (\omega c + \omega \alpha)t - In \cos (\omega c - \omega \alpha)t + Qn \sin (\omega c - \omega \alpha)t \end{aligned} \tag{5}$$

[0027] Next, AM-synchronous detection for the AM data multiplex modulated signal generated in the above manner will be described.

[0028] For synchronous detection, the equation (5) is multiplied by the carrier cos ωct to obtain the following equation:

$$\begin{gathered} 2\{v(t) \cos \omega ct\} = \{1 + \kappa vm(t)\} + In \cos \omega \alpha t + Qn \sin \omega \alpha t \\ - In \cos(-\omega \alpha)t + Qn \sin(-\omega \alpha)t + \{1 + \kappa vm(t)\} \cos 2\omega ct + In \cos (2\omega c + \omega \alpha)t \\ + Qn \sin (2\omega c + \omega \alpha)t - In \cos (2\omega c - \omega \alpha)t + Qn \sin (2\omega c - \omega \alpha)t \end{gathered}$$

[0029] The AM synchronous detector has a low-pass filter so that high frequency components are removed. Therefore, the above equation is changed to the following equation (6):

$$\begin{aligned} 2\{v(t)\cos\omega ct\} &= \{1+\kappa vm(t)\} + In\cos\omega\alpha t + Qn\sin\omega\alpha t - In\cos\omega\alpha t - Qn\sin\omega\alpha t \\ &= \{1+\kappa vm(t)\} + In\cos\omega\alpha t + Qn\sin\omega\alpha t - In\cos(-\omega\alpha)t + Qn\sin(-\omega\alpha)t \\ &= 1+\kappa vm(t) \end{aligned} \qquad (6).$$

[0030] As seen from the equation (6), the digital modulated signal components are canceled out. Therefore, if the d.c. component of the equation (6) is cut and the left signal is amplified, the original signal vm(t) before it is modulated by the AM data multiplex modulated signal generating apparatus of the embodiment can be picked up. It can, therefore, be understood that an AM-synchronous detection signal obtained by AM-synchronous detecting the AM data multiplex modulated signal modulated by the AM multiplex modulated signal generator shown in Fig. 2 is not adversely affected.

[0031] The QPSK baseband digital signal generator 12 shown in Fig. 2 may use other modulation methods, such as PSK, ASK, QAM, FSK, MSK, or the like. Although the embodiment uses two digital modulation carriers at frequencies (fc + fα) and (fc - fα), two or more digital modulation carriers may also be used, such as multi-carriers, frequency hopping, OFDM, or the like.

[0032] The AM data multiplex modulated signal modulated in the above manner is obtained by multiplexing the digital modulated signal and the AM modulated signal in the same frequency band and at the same time. Therefore, as different from those modulation methods of time division multiplex and frequency multiplex, the cock signal cannot be reproduced by extracting a desired digital modulated signal at a selected data multiplex time and frequency band.

[0033] As shown in Fig. 1, in the clock regeneration circuit according to the embodiment of the invention, an AM data multiplex modulated signal is supplied to a band-pass filter 1 having a narrower band than the band width of the AM data multiplex modulated signal to extract the carrier of the AM modulated signal. The extracted carrier is supplied to a limiter 2 to remove AM modulated components which are not removed by the band-pass filter 1. An output of the limiter 2 is supplied to a phase comparator 3.

[0034] An output of the phase comparator 3 is supplied to a loop filter 4 composed of a low-pass filter to smooth it which is then supplied to a voltage-controlled oscillator 5 as a frequency control voltage. A free-running oscillation frequency of an oscillation output of the voltage-controlled oscillator 5 is set to 32 MHz. An oscillation output of the voltage-controlled oscillator 5 is output as a regenerated clock signal and also supplied to a direct digital synthesizer 6.

[0035] In the direct digital synthesizer 6, the oscillation output of the voltage-controlled oscillator 5 is frequency-divided into a signal having a frequency of 2 MHz, a frequency-divided signal output from the frequency divider 61 being supplied to a counter 62. Waveform data is read from a waveform ROM 63 which stores waveforms, by using a count of the counter as an address. The waveform data read from the waveform ROM is supplied to a D/A converter 64 in which it is converted into an analog signal. This analog signal is supplied to a low-pass filter 7 to remove aliasing components, and thereafter supplied to the phase comparator 3. The D/A converter 64 is supplied with an output from the frequency divider 61 as its conversion clock signal. -

[0036] In this embodiment, even if the oscillation frequency of 32 MHz of the voltage-controller oscillator 5 is not an integer multiple (division ratio of the frequency divider 61) of an input frequency (reception frequency, such as 954 kHz, 1242 kHz, or the like, or an intermediate frequency) and has a fraction of the integer multiple, a regenerated clock signal can be obtained which has a predetermined regeneration clock frequency. It is, therefore, possible to obtain a regenerated clock signal having a predetermined regenerated clock frequency, by using the direct digital synthesizer having the waveform data ROM 63. It is necessary to set the input frequency in advance. Therefore, the waveform data ROM 63 stores sine wave data having input frequencies. In accordance with the input frequency, waveform data corresponding to the count of the counter 62 is read from the waveform data ROM 63 and converted into analog data which is input to the phase comparator. Namely, the direct digital synthesizer is used in order to obtain a predetermined regeneration clock by storing in advance waveform data corresponding to input frequencies.

[0037] In the clock reproduction circuit constructed as above according to the embodiment of the invention, the band-pass filter 1 extracts the carrier of the AM modulated signal from the AM data multiplex modulated signal, AM modulated components of the extracted carrier which are not removed by the band-pass filter 1 are removed by the limiter 2, and the carrier is supplied to the phase comparator 3 as a reference signal.

[0038] An output of the phase comparator 3 is smoothed by the loop filter 4, and the oscillation frequency of the voltage-controlled oscillator 5 is controlled in accordance with an output of the loop filter 4. The free-running oscillation frequency of an oscillation output of the voltage-controlled oscillator 5 is set to 32 MHz. An oscillation output of the voltage-controlled oscillator 5 is frequency-divided by the direct digital synthesizer 6, the frequency-divided signal is counted, and waveform data is read from the waveform data ROM 63 in accordance with a count value of the counter 62. The waveform data is converted into an analog signal by the D/A converter 64, and supplied via the low-pass filter 7 to the phase comparator 3 in which it is compared with the carrier of the AM modulated signal.

[0039] If the frequency of an output signal from the D/A converter 64 is different from the carrier frequency of the AM modulated signal, a beat corresponding to the frequency difference is superposed upon an output of the loop filter 4 so that the oscillation frequency of the voltage-controlled oscillator 5 changes. Accordingly, the carrier frequency of the AM modulated signal and the output signal of the low-pass filter 7 via the D/A converter 64 are synchronized with the carrier of the AM modulated signal.

[0040] An oscillation output from the voltage-controlled oscillator 5 therefore, becomes, a clock signal synchronized with the carrier of the AM modulated signal, and the oscillation output from the voltage-controlled oscillator 5 can be used as a clock signal for demodulating a digital modulated signal separated from the AM data multiplex modulated signal.

[0041] In the clock regeneration circuit according to the embodiment of the invention described above, the direct digital synthesizer 6 is used by way of example. Instead of the direct digital synthesizer 6, other frequency dividers may also be used. Also, in the clock regeneration circuit according to the embodiment of the invention described above, although QPSK is used as a digital modulation method, other modulation methods such as PSK, ASK, QAM, FSK and MSK may also be used, with similar advantages being expected.

SECOND EMBODIMENT

[0042] A clock regeneration circuit according to another embodiment of the invention is shown in Fig. 4. Referring to Fig. 4, an AM data multiplex modulated signal is supplied to a frequency converter 201 to be converted into an intermediate frequency. The AM data multiplex modulated signal converted into the intermediate frequency is band-limited by a band-pass filter 202 having a narrower band than the band width of the AM data multiplex modulated signal. The band-pass filter 202 extracts the carrier of the AM modulated signal from the AM data multiplex modulated signal.

[0043] The carrier extracted by the band-pass filter 202 is further supplied to a limiter 203 in which AM modulated components which are not removed by the band-pass filter 202 are removed. An output of the limiter 203 is supplied to a phase comparator 204. An output of the phase comparator 204 is supplied to a loop filter 205 composed of a low-pass filter to smooth the output of the phase comparator which is supplied to a voltage-controlled oscillator 206 as a frequency control signal. An oscillation output of the voltage-controlled oscillator 206 is output as a regenerated clock signal and also supplied to a direct digital synthesizer 207.

[0044] The direct digital synthesizer 207 outputs waveform data having a frequency equal to the frequency-converted carrier frequency, for example, in accordance with an oscillation output of the voltage-controlled oscillator 206. The waveform data output from the direct digital synthesizer 207 is supplied to a D/A converter 208 to be converted into an analog signal. The frequency of the converted analog signal is equal to the frequency-converted carrier frequency, and after aliasing components of the analog signal are removed at a low-pass filter 209, the signal is supplied to the phase comparator 204. In accordance with an output from the phase comparator 204, the oscillation frequency of the voltage-controlled oscillator 206 is controlled.

[0045] An oscillation output from the voltage-controlled oscillator 206 is also supplied to another direct digital synthesizer 210 which outputs waveform data having a frequency equal to the local oscillation frequency. The waveform data output from the direct digital synthesizer 210 is supplied to a D/A converter 211 to be converted into an analog signal. The frequency of the converted analog signal is equal to the local oscillation frequency, and after aliasing components of the analog signal are removed at a low-pass filter 212, the signal is supplied to the frequency converter 201 as a local oscillation output to thereby convert the AM data multiplex modulated signal into an intermediate frequency.

[0046] In the clock regeneration circuit constructed as above according to the second embodiment of the invention, the AM data multiplex modulated signal is converted into the intermediate frequency, the band-pass filter 202 extracts the carrier of the AM modulated signal from the AM data multiplex modulated signal converted into the intermediate frequency, AM modulated components of the extracted carrier which are not removed by the band-pass filter 202 are removed by the limiter 203, and the carrier is supplied to the phase comparator 204 as a reference signal.

[0047] An output of the phase comparator 204 is smoothed by the loop filter 205, and the oscillation frequency of the voltage-controlled oscillator 206 is controlled in accordance with an output of the loop filter 205. An oscillation output of the voltage-controlled oscillator 205 is supplied to the direct digital synthesizer 207 which outputs the waveform data having a frequency equal to the frequency-converted carrier frequency. The waveform data is converted into an analog signal by the D/A converter 208, and after aliasing noises are removed by the low-pass filter 209, the phase of the analog signal is compared by the phase comparator 204 with the carrier of the frequency-converted AM modulated signal output from the limiter 203.

[0048] If the frequency of an output signal from the D/A converter 208 is different from the carrier frequency of the frequency-converted AM modulated signal, a beat corresponding to the frequency difference is superposed upon an output of the loop filter 205 so that the oscillation frequency of the voltage-controlled oscillator 206 is changed. Accordingly, the frequencies of the waveform data output from the direct digital synthesizers 207 and 210 are changed so that the frequencies of the output signals from the D/A converters 208 and 211 are changed. Therefore, the output signal

via the low-pass filter 209 from the D/A converter 208 converges to the carrier frequency of the frequency-converted AM modulated signal, and then the output signal via the low-pass filter 212 from the D/A converter 211 converges to the local oscillation frequency used for frequency conversion. Accordingly, the oscillation frequency of the voltage-controlled oscillator 206 is synchronized with the carrier of the frequency-converted AM modulated signal.

[0049] An oscillation output from the voltage-controlled oscillator 106 therefore, becomes, a clock signal synchronized with the carrier of the AM modulated signal, and the oscillation output from the voltage-controlled oscillator 206 can be used as a clock signal for demodulating a digital modulated signal separated from the AM data multiplex modulated signal.

[0050] As described so far, according to the clock regeneration circuit of the invention, it is possible to regenerate a clock signal for data demodulation from an AM data multiplex modulated signal obtained by multiplexing a digital modulated signal and an AM modulated signal in the same frequency band and at the same time.

Claims

1. A clock regeneration circuit for regenerating a clock signal for data demodulation from an AM data multiplex modulated signal obtained by multiplexing a digital modulated signal and an AM modulated signal in the same frequency band and at the same time, the clock regeneration circuit comprising, carrier extracting means for extracting a carrier of the AM modulated signal from the AM data multiplex modulated signal, phase comparator means for receiving as one input the carrier extracted by said carrier extracting means, a voltage-controlled oscillator whose oscillation frequency is controlled by an output from said phase comparator means, and frequency-dividing means for frequency-dividing the oscillation frequency of said voltage-controlled oscillator and supplying a frequency-divided output to said phase comparator means as another input, wherein the oscillation output of said voltage-controlled oscillator is a clock signal synchronized with the carrier of the AM data multiplex modulated signal.

2. A clock regeneration circuit according to claim 1, wherein said frequency-dividing means includes a direct digital synthesizer.

3. A clock regeneration circuit according to claim 2, wherein said direct digital synthesizer includes a counter and a waveform ROM.

4. A clock regeneration circuit according to claim 1 further comprising a loop filter for smoothing an output of said phase comparator means and applying the smoothed output to said voltage-controlled oscillator.

5. A clock regeneration circuit for regenerating a clock signal for data demodulation from an AM data multiplex modulated signal obtained by multiplexing a digital modulated signal and an AM modulated signal in the same frequency band and at the same time, the clock regeneration circuit comprising, frequency-converting means for frequency-converting the AM data multiplex modulated signal into an intermediate frequency, carrier extracting means for extracting a carrier of the AM modulated signal from the AM data multiplex modulated signal frequency-converted into the intermediate frequency, phase comparator means for receiving as one input the carrier extracted by said carrier extracting means, a voltage-controlled oscillator whose oscillation frequency is controlled by an output from said phase comparator means, a first direct digital synthesizer for inputting an oscillation output from said voltage-controlled oscillator and supplying an output to said phase comparator means as another input, and a second direct digital synthesizer for inputting the oscillation output from said voltage-controlled oscillator and supplying an output to said frequency-converting means as a local oscillation output, wherein the oscillation output of said voltage-controlled oscillator which is a clock signal synchronized with the carrier of the AM data multiples modulated signal is used as a clock signal for data demodulation from the AM data multiplex modulated signal.

FIG. 1

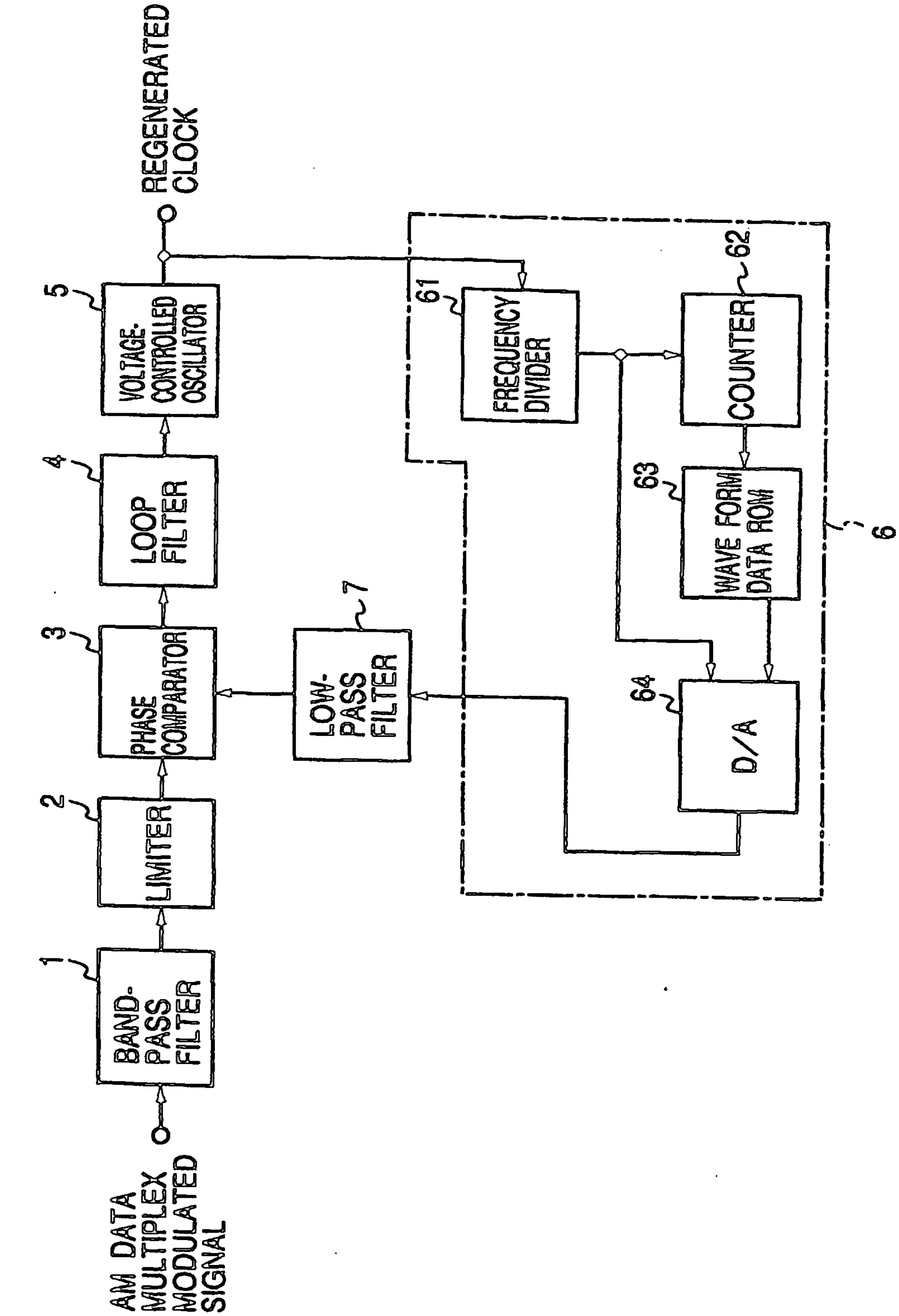

AM DATA MULTIPLEX MODULATED SIGNAL
BAND-PASS FILTER
1
LIMITER
2
PHASE COMPARATOR
3
LOOP FILTER
4
VOLTAGE-CONTROLLED OSCILLATOR
5
REGENERATED CLOCK
LOW-PASS FILTER
7
FREQUENCY DIVIDER
61
COUNTER
62
WAVE FORM DATA ROM
63
D/A
64
6

FIG. 2

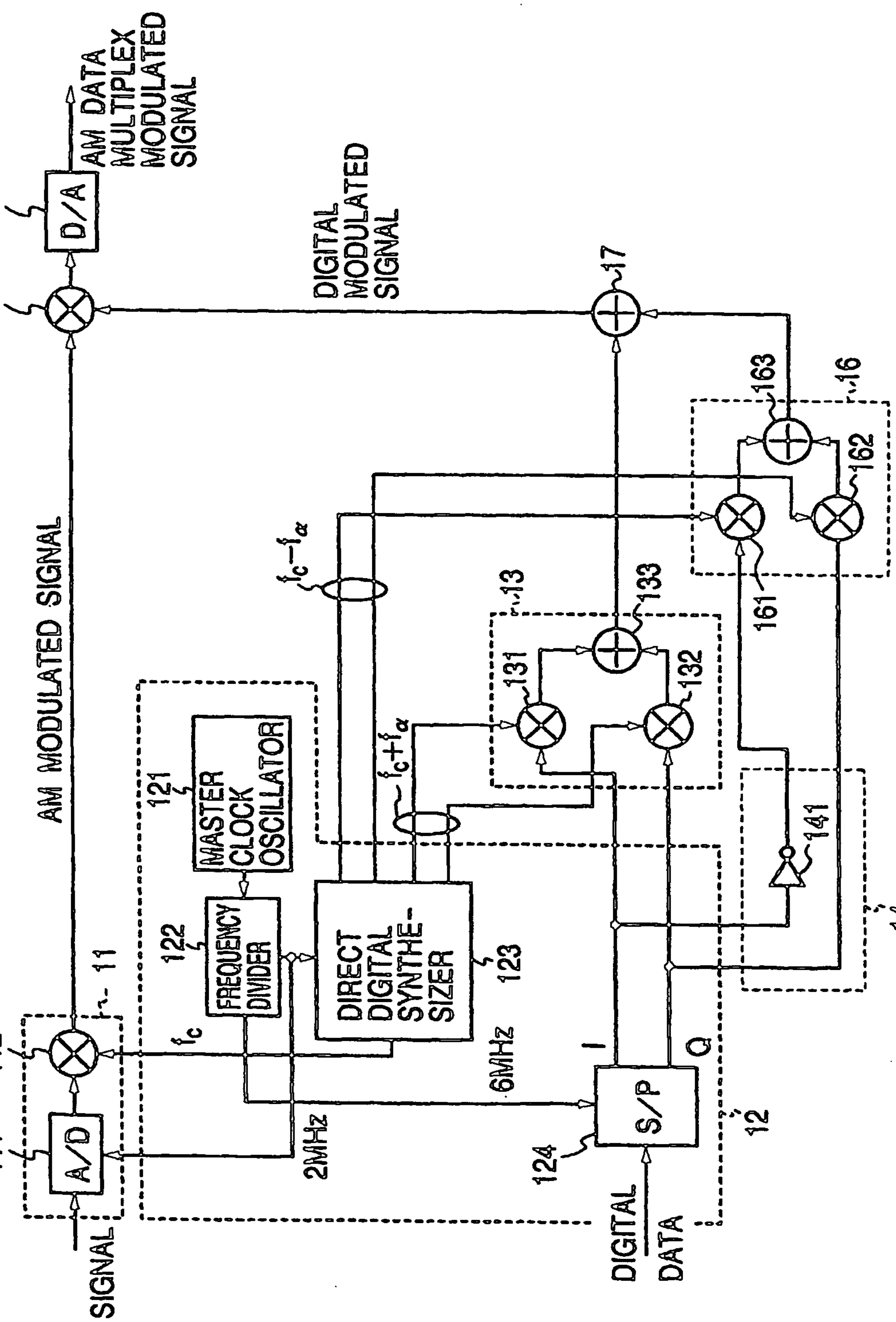

AM MODULATED SIGNAL
SIGNAL
111
A/D
112
11
2MHz
fc
121
MASTER CLOCK OSCILLATOR
122
FREQUENCY DIVIDER
DIRECT DIGITAL SYNTHE-SIZER
123
6MHz
124
S/P
I
Q
12
DIGITAL DATA
fc+fα
fc−fα
131
132
133
13
141
14
161
162
163
16
17
18
DIGITAL MODULATED SIGNAL
20
D/A
AM DATA MULTIPLEX MODULATED SIGNAL

FIG. 3

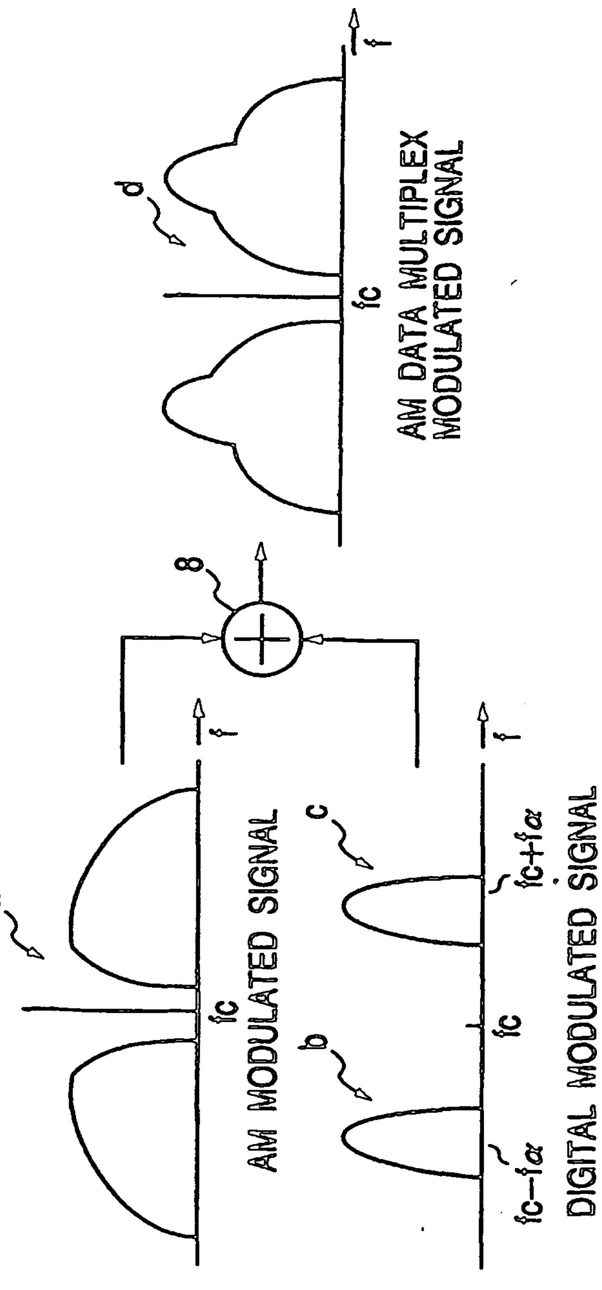
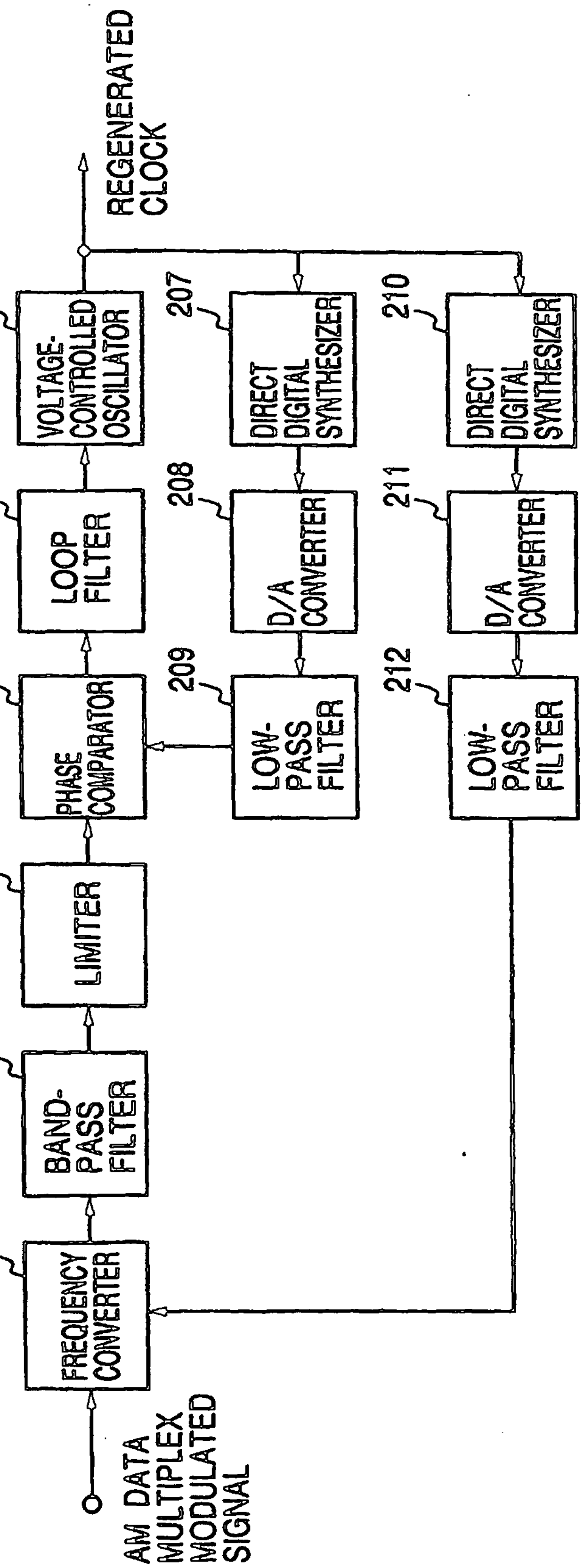

a
fc
f
AM MODULATED SIGNAL
b
c
fc−fα
fc
fc+fα
f
DIGITAL MODULATED SIGNAL
8
d
fc
f
AM DATA MULTIPLEX
MODULATED SIGNAL

FIG. 4


AM DATA MULTIPLEX MODULATED SIGNAL
201
FREQUENCY CONVERTER
202
BAND-PASS FILTER
203
LIMITER
204
PHASE COMPARATOR
205
LOOP FILTER
206
VOLTAGE-CONTROLLED OSCILLATOR
REGENERATED CLOCK
207
DIRECT DIGITAL SYNTHESIZER
208
D/A CONVERTER
209
LOW-PASS FILTER
210
DIRECT DIGITAL SYNTHESIZER
211
D/A CONVERTER
212
LOW-PASS FILTER

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/02553

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl^6 H04L27/22, H04J9/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl^6 H04L27/00-27/38, H04J9/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1940-1998
Kokai Jitsuyo Shinan Koho 1971-1998

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, A	JP, 9-326836, A (Kenwood Corp.), 16 December, 1997 (16. 12. 97) (Family: none)	1-5
P, A	JP, 10-22974, A (Kenwood Corp.), 23 January, 1998 (23. 01. 98) (Family: none)	1-5
P, A	JP, 10-22956, A (Kenwood Corp.), 23 January, 1998 (23. 01. 98) (Family: none)	1-5
A	JP, 9-102775, A (Ikegami Tsushinki Co., Ltd.), 15 April, 1997 (15. 04. 97) (Family: none)	1-5
A	JP, 7-202965, A (NEC Corp.), 4 August, 1995 (04. 08. 95) (Family: none)	1-5
A	JP, 7-58636, A (Fujitsu Ltd.), 3 March, 1995 (03. 03. 95), Fig. 2 (Family: none)	1-5

[x] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/02553

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 5-122063, A (NEC Corp.), 18 May, 1993 (18. 05. 93), Fig. 6 & EP, 538903, A1 & US, 5329253, A	1-5

CLOCK REGENERATION CIRCUIT

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JP9326836
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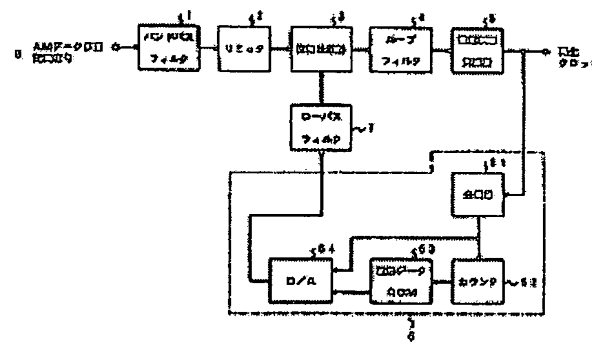
Abstract of WO9857470

A clock regeneration circuit for regenerating a clock signal for demodulating data from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of an amplitude-modulated signal at the same time. The carrier for an amplitude-modulated signal is extracted from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of the amplitude-modulated signal at the same time through a band-pass filter (1), and the oscillation frequency of a voltage-controlled oscillator (5) is controlled by the output of a phase comparator (3) through a loop filter (4). The oscillation output of the voltage-controlled oscillator (5) is supplied to a direct digital synthesizer (6) and the phase of the carrier extracted through the band-pass filter (1) is compared with the phase of the output of the direct digital synthesizer (6) by means of the phase comparator (3). The oscillation output of the voltage-controlled oscillator (5) is then synchronized with the carrier for the amplitude-modulated signal to produce a



1 ... Band-pass filter
2 ... Limiter
3 ... Phase comparator
4 ... Loop filter
5 ... Voltage-controlled oscillator
61 ... Frequency divider
62 ... Counter
63 ... Waveform data ROM
7 ... Low-pass filter
a ... AM data multiplex modulated signal
b ... Regenerated clock

CLOCK REGENERATION CIRCUIT

Description of correspondent: EP0989706

TECHNICAL FIELD

[0001] The present invention relates to a clock regeneration circuit for regenerating a clock signal for data demodulation from an AM data multiplex demodulated signal which is obtained by multiplexing a digital modulated signal and an AM modulated signal in the same frequency band and at the same time.

RELATED BACKGROUND ART

[0002] A conventional data multiplex method is roughly classified into a time division multiplex method used by character multiplex broadcasting of television broadcasting and a frequency multiplex method used by character multiplex broadcasting used by FM broadcasting. The frequency band occupied by AM broadcasting is narrow so that frequency multiplex and time division multiplex cannot be used. An AM data multiplex modulated signal generating apparatus for multiplexing an AM modulated signal and a digital modulated signal in the manner similar to data multiplex broadcasting in television or FM broadcasting, has not been realized as yet.

[0003] The applicant of the present application has proposed an apparatus for generating an AM data multiplex modulated signal to be obtained by multiplexing an AM modulated signal and a digital modulated signal, the apparatus not adversely affecting an AM synchronous detection output when the AM data multiplex modulated signal is AM-synchronously detected (JP-A-8-166636).

[0004] The specific contents of an AM data multiplex modulated signal modulated in the above manner will be later detailed. Since a digital modulated signal and an AM modulated signal are multiplexed in the same frequency band and at the same time, a modulating method is different from that used by time division multiplexing or frequency multiplexing. It is, therefore, impossible to reproduce a clock signal used for signal demodulation through synchronous detection, by extracting a desired digital modulated signal at a selected data multiplex time and frequency band as in conventional cases.

SUMMARY OF THE INVENTION

[0005] It is an object of the present invention to provide a clock regeneration circuit for regenerating a clock signal used for data demodulation from an AM data

digital modulated signal in the same frequency band and at the same time.

[0006] According to one aspect of the present invention, a clock regeneration circuit for regenerating a clock signal for data demodulation from an AM data multiples modulated signal obtained by multiplexing a digital modulated signal and an AM modulated signal in the same frequency band and at the same time, comprises carrier extracting means for extracting a carrier of the AM modulated signal from the AM data multiplex modulated signal, phase comparator means for receiving as one input the carrier extracted by the carrier extracting means, a voltage-controlled oscillator whose oscillation frequency is controlled by an output from the phase comparator means, and frequency-dividing means for frequency-dividing the oscillation frequency of the voltage-controlled oscillator and supplying a frequency-divided output to the phase comparator means as another input.

[0007] In the clock regeneration circuit of this invention, the carrier extracting means extracts the carrier of the AM modulated signal from the AM data multiplex modulated signal, the phases of the extracted carrier and an output of the frequency divider are compared by the phase comparator, and in accordance with a phase comparison result, the oscillation frequency of the voltage-controlled oscillator is controlled. Accordingly, the oscillation output of the voltage-controlled oscillator is synchronized with the carrier of the AM modulated signal, and the oscillation output of the voltage-controlled oscillator can be used as the clock signal for demodulating the digital modulated signal separated from the AM data multiplex modulated signal.

[0008] As the frequency divider, a direct digital synthesizer may be used which is input with an oscillation output from the voltage-controlled oscillator and supplies an output to the phase comparator as the other input.

[0009] According to another aspect of the invention, a clock regeneration circuit for regenerating a clock signal for data demodulation from an AM data multiplex modulated signal obtained by multiplexing a digital modulated signal and an AM modulated signal in the same frequency band and at the same time, comprises frequency-converting means for frequency-converting the AM data multiplex modulated signal into an intermediate frequency, carrier extracting means for extracting a carrier of the AM modulated signal from the AM data multiplex modulated signal frequency-converted into the intermediate frequency, phase comparator means for receiving as one input the carrier extracted by the carrier extracting means, a voltage-controlled oscillator whose oscillation frequency is controlled by an output from the phase comparator means, and a first direct digital synthesizer for inputting an oscillation output from the voltage-controlled oscillator and supplying an output to the phase comparator means as another input, and a second direct digital synthesizer for inputting the oscillation output from the voltage-controlled oscillator and supplying an output to the frequency-converting means as a local oscillation output, wherein the oscillation output of the voltage-controlled oscillator is used as a clock signal for data demodulation from the AM data multiplex modulated signal.

[0010] According to this clock regeneration circuit of this invention, the carrier extracting means extracts the carrier of the AM modulated signal from the

extracted carrier and an output of the first direct digital synthesizer are compared by the phase comparator, and in accordance with a phase comparison result, the oscillation frequency of the voltage-controlled oscillator is controlled. The oscillation output of the voltage-controlled oscillator is supplied to the frequency-converting means as a local oscillation output. Accordingly, the oscillation output of the voltage-controlled oscillator is synchronized with the carrier of the AM modulated signal, and the oscillation output of the voltage-controlled oscillator can be used as the clock signal for demodulating the digital modulated signal separated from the AM data multiplex modulated signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Fig. 1 is a block diagram showing the structure of a clock regeneration circuit according to an embodiment of the invention, Fig. 2 is a block diagram showing the structure of an AM data multiplex modulated signal generating apparatus used for explaining the clock regeneration circuit of the embodiment, Fig. 3 is a schematic diagram illustrating the operation of the AM data multiplex modulated signal generating apparatus shown in Fig. 2, and Fig. 4 is a block diagram showing the structure of a clock regeneration circuit according to another embodiment of the invention.

EMBODIMENTS OF THE INVENTION

FIRST EMBODIMENT

[0012] A clock regeneration circuit of this invention will be described with reference to preferred embodiments. Fig. 1 is a block diagram showing the structure of a clock regeneration circuit according to a first embodiment of the invention.

[0013] Prior to describing the clock regeneration circuit of the invention, an apparatus for generating an AM data multiplex modulated signal will be described with reference to Fig. 2.

[0014] In the AM data multiplex modulated signal generating apparatus, an analog signal (hereinafter simply called an input signal where applicable), such as a voice signal or the like is supplied to an AM modulator 11 in which the input signal is AM-modulated by a carrier having a frequency of fc generated by a frequency divider 112 to be later described. The AM modulator 11 is composed of an A/D converter 111 for A/D converting the input signal and a multiplier 112 for AM-modulating an output of the A/D converter 111.

[0015] The AM data multiplex modulated signal generating apparatus also includes a QPSK baseband signal generator 12 which is composed of: a master clock oscillator 121 for oscillating at a frequency of, e.g., 32 MHz; a frequency divider

generate signals having frequencies of 2 MHz and 6 kHz; a direct digital synthesizer 123 for receiving a signal having a frequency of 2 MHz from the frequency divider 122 and generating the carrier having the frequency of fc, two orthogonal signals having a frequency of (fc + f alpha) and two orthogonal signals having a frequency of (fc - f alpha); and a serial/parallel converter 124 for converting serial digital data I and Q of 6 kbps into parallel digital data I and Q. The QPSK baseband digital signal generator 12 outputs QPSK baseband digital signals from the serial/parallel converter 124. An output signal having a frequency of 2 MHz is used as a clock signal for the A/D converter 111, an output signal having a frequency fc is supplied as a clock signal of the AM modulator 112, and an output signal having a frequency of 6 kHz is supplied as a conversion clock signal of the serial/parallel converter 124.

[0016] The QPSK baseband digital signals I and Q output from the QPSK baseband digital signal generator 12 are supplied to a quadrature modulator 13 composed of multipliers 131 and 132 and an adder 133. The multiplier 131 multiplies the I data by cos (omega c + omega alpha)t, the multiplier 132 multiplies the Q data by sin (omega c + omega alpha)t, and the adder 133 adds the outputs of the multipliers 131 and 132 to thereby quadrature-modulate the carrier having a frequency of (fc + f alpha) by the QPSK baseband digital signals. The frequencies (fc + f alpha) and (fc - f alpha) correspond to the frequencies of upper and lower AM modulated side bands.

[0017] The QPSK baseband digital signals I and Q output from the QPSK baseband digital signal generator 12 are also supplied to a complex conjugator 14 which generates a complex conjugate of sign inverted digital signals I and Q. The complex conjugator 14 may be composed of an inverter 141 for inverting the I signal.

[0018] The QPSK baseband digital signals I and Q output from the complex conjugator 14 are supplied to a quadrature modulator 16 composed of multiplies 161 and 162 and an adder 163. The multiplier 161 multiplies the I data by cos (omega c - omega alpha)t, the multiplier 162 multiplies the Q data by sin (omega c - omega alpha)t, and the adder 163 adds the outputs of the multipliers 161 and 162 to thereby quadrature-modulate the carrier having a frequency of (fc - f alpha) by the QPSK baseband digital signals I and Q output from the complex conjugator 14. Output signals from the quadrature modulators 13 and 16 are added by an adder 17. An output signal from the adder 17, i.e., a digital modulated signal and an AM modulated signal output from the AM modulator are added by an adder 18. An addition signal from the adder 18 is supplied to a D/A converter 20 to convert it into an analog signal which is output as an AM data multiplex modulated signal.

[0019] An AM data multiplex modulation process by the AM data multiplex modulated signal generating apparatus shown in Fig. 2 and structured as above is schematically illustrated in Fig. 3. Referring to Fig. 3, an AM modulated signal output from the AM modulator 1 is indicated at a in Fig. 3. An output signal of the quadrature modulator 16, i.e., a digital modulated signal, is indicated at b in Fig. 3, and an output signal of the quadrature modulator 13, i.e., a digital modulated signal, is indicated at c in Fig. 3. A digital modulated signal output from the adder 17 is a sum of b and c shown in Fig. 3, and the AM data multiplex modulated signal

[0020] An AM data multiplex modulation process by the AM data multiplex modulated signal generating apparatus shown in Fig. 2 will be described.

[0021] An AM modulated signal nu AM(t) is expressed by the following equation (1):
"(1)" nu AM(t) = {I + kappa nu m(t)} cos omega ct
where I is an amplitude of the carrier, omega c (rad/s) is an angular frequency of the carrier, kappa is a modulation factor, and nu m(t) is an input signal.

[0022] The I and Q signal trains generated by the QPSK baseband digital signal generator 12 are represented by In and Qn which are also called dibits, where

In = +/- 1

Qn = +/- 1.

[0023] The output signals from the QPSK baseband digital signal generator 12 are branched, one being supplied to the quadrature modulator 13 to which the carrier having the frequency (fc + f alpha) is supplied, whereat the carrier having an angular velocity of (omega c + omega alpha) (rad/s) is quadrature-modulated by the complex signal train. An output signal nu DH(t) of the quadrature modulator 13 is expressed by the following equation (2):
"(2)." nu DH(t) = In cos (omega c + omega alpha)t + Qn sin (omega c + omega alpha)t

[0024] The other output signal from the QPSK baseband digital signal generator 12 is supplied to the quadrature modulator 14 in which the signs of the output signals In and Qn are converted into (-In) and (Qn). This complex signal train is supplied to the quadrature modulator 16 to which the carrier having the frequency (fc - f alpha) is supplied, whereat the carrier having an angular velocity of (omega c - omega alpha) (rad/s) is quadrature-modulated by the complex signal train. An output signal nu DL(t) of the quadrature modulator 16 is expressed by the following equation (3):
"(3)." nu DL(t) = - In cos (omega c - omega alpha)t + Qn sin (omega c - omega alpha)t

[0025] The output signals nu DH(t) and nu DL(t) given by the equations (2) and (3) are added by the adder 17, and the addition signal or digital modulated signal nu D (t) is given by the following equation (4):
"(4)." nu D(t) = nu DH(t) + nu DL(t)
= In cos (omega c + omega alpha)t + Qn sin (omega c + omega alpha)t - In cos (omega c - omega alpha)t + Qn sin (omega c - omega alpha)t

[0026] The AM modulated signal nu AM(t) and digital modulated signal nu D(t) are

expressed by the following equation (5) by using the equations (1) and (4):
"(5)" nu (t) = nu AM(t) + nu D(t)
= {l + kappa nu m(t)} cos omega ct + In cos (omega c + omega alpha)t + Qn sin (omega c + omega alpha)t - In cos (omega c - omega alpha)t + Qn sin (omega c - omega alpha)t

[0027] Next, AM-synchronous detection for the AM data multiplex modulated signal generated in the above manner will be described.

[0028] For synchronous detection, the equation (5) is multiplied by the carrier cos omega ct to obtain the following equation:
2 { nu (t) cos omega ct} = {1 + kappa nu m(t)} + In cos omega alpha t + Qn sin omega alpha t - In cos(- omega alpha)t + Qn sin(- omega alpha)t + {1 + kappa nu m(t)} cos 2 omega ct + In cos (2 omega c + omega alpha)t + Qn sin (2 omega c + omega alpha)t - In cos (2 omega c - omega alpha)t + Qn sin (2 omega c - omega alpha)t

[0029] The AM synchronous detector has a low-pass filter so that high frequency components are removed. Therefore, the above equation is changed to the following equation (6):
"(6)." 2 { nu (t) cos omega ct} = {1 + kappa nu m(t)} + In cos omega alpha t + Qn sin omega alpha t - In cos(- omega alpha)t + Qn sin(- omega alpha)t
= {1 + kappa nu m(t)} + In cos omega alpha t + Qn sin omega alpha t - In cos omega alpha t - Qn sin omega alpha t
= 1 + kappa nu m(t)

[0030] As seen from the equation (6), the digital modulated signal components are canceled out. Therefore, if the d.c. component of the equation (6) is cut and the left signal is amplified, the original signal nu m(t) before it is modulated by the AM data multiplex modulated signal generating apparatus of the embodiment can be picked up. It can, therefore, be understood that an AM-synchronous detection signal obtained by AM-synchronous detecting the AM data multiplex modulated signal modulated by the AM multiplex modulated signal generator shown in Fig. 2 is not adversely affected.

[0031] The QPSK baseband digital signal generator 12 shown in Fig. 2 may use other modulation methods, such as PSK, ASK, QAM, FSK, MSK, or the like. Although the embodiment uses two digital modulation carriers at frequencies (fc + f alpha) and (fc - f alpha), two or more digital modulation carriers may also be used, such as multi-carriers, frequency hopping, OFDM, or the like.

[0032] The AM data multiplex modulated signal modulated in the above manner is obtained by multiplexing the digital modulated signal and the AM modulated signal in the same frequency band and at the same time. Therefore, as different from those modulation methods of time division multiplex and frequency multiplex, the cock signal cannot be reproduced by extracting a desired digital modulated signal at a selected data multiplex time and frequency band.

[0033] As shown in Fig. 1, in the clock regeneration circuit according to the embodiment of the invention, an AM data multiplex modulated signal is supplied to a band-pass filter 1 having a narrower band than the band width of the AM data multiplex modulated signal to extract the carrier of the AM modulated signal. The extracted carrier is supplied to a limiter 2 to remove AM modulated components which are not removed by the band-pass filter 1. An output of the limiter 2 is supplied to a phase comparator 3.

[0034] An output of the phase comparator 3 is supplied to a loop filter 4 composed of a low-pass filter to smooth it which is then supplied to a voltage-controlled oscillator 5 as a frequency control voltage. A free-running oscillation frequency of an oscillation output of the voltage-controlled oscillator 5 is set to 32 MHz. An oscillation output of the voltage-controlled oscillator 5 is output as a regenerated clock signal and also supplied to a direct digital synthesizer 6.

[0035] In the direct digital synthesizer 6, the oscillation output of the voltage-controlled oscillator 5 is frequency-divided into a signal having a frequency of 2 MHz, a frequency-divided signal output from the frequency divider 61 being supplied to a counter 62. Waveform data is read from a waveform ROM 63 which stores waveforms, by using a count of the counter as an address. The waveform data read from the waveform ROM is supplied to a D/A converter 64 in which it is converted into an analog signal. This analog signal is supplied to a low-pass filter 7 to remove aliasing components, and thereafter supplied to the phase comparator 3. The D/A converter 64 is supplied with an output from the frequency divider 61 as its conversion clock signal. -

[0036] In this embodiment, even if the oscillation frequency of 32 MHz of the voltage-controller oscillator 5 is not an integer multiple (division ratio of the frequency divider 61) of an input frequency (reception frequency, such as 954 kHz, 1242 kHz, or the like, or an intermediate frequency) and has a fraction of the integer multiple, a regenerated clock signal can be obtained which has a predetermined regeneration clock frequency. It is, therefore, possible to obtain a regenerated clock signal having a predetermined regenerated clock frequency, by using the direct digital synthesizer having the waveform data ROM 63. It is necessary to set the input frequency in advance. Therefore, the waveform data ROM 63 stores sine wave data having input frequencies. In accordance with the input frequency, waveform data corresponding to the count of the counter 62 is read from the waveform data ROM 63 and converted into analog data which is input to the phase comparator. Namely, the direct digital synthesizer is used in order to obtain a predetermined regeneration clock by storing in advance waveform data corresponding to input frequencies.

[0037] In the clock reproduction circuit constructed as above according to the embodiment of the invention, the band-pass filter 1 extracts the carrier of the AM modulated signal from the AM data multiplex modulated signal, AM modulated components of the extracted carrier which are not removed by the band-pass filter 1 are removed by the limiter 2, and the carrier is supplied to the phase comparator 3 as a reference signal.

[0038] An output of the phase comparator 3 is smoothed by the loop filter 4, and

accordance with an output of the loop filter 4. The free-running oscillation frequency of an oscillation output of the voltage-controlled oscillator 5 is set to 32 MHz. An oscillation output of the voltage-controlled oscillator 5 is frequency-divided by the direct digital synthesizer 6, the frequency-divided signal is counted, and waveform data is read from the waveform data ROM 63 in accordance with a count value of the counter 62. The waveform data is converted into an analog signal by the D/A converter 64, and supplied via the low-pass filter 7 to the phase comparator 3 in which it is compared with the carrier of the AM modulated signal.

[0039] If the frequency of an output signal from the D/A converter 64 is different from the carrier frequency of the AM modulated signal, a beat corresponding to the frequency difference is superposed upon an output of the loop filter 4 so that the oscillation frequency of the voltage-controlled oscillator 5 changes. Accordingly, the carrier frequency of the AM modulated signal and the output signal of the low-pass filter 7 via the D/A converter 64 are synchronized with the carrier of the AM modulated signal.

[0040] An oscillation output from the voltage-controlled oscillator 5 therefore, becomes, a clock signal synchronized with the carrier of the AM modulated signal, and the oscillation output from the voltage-controlled oscillator 5 can be used as a clock signal for demodulating a digital modulated signal separated from the AM data multiplex modulated signal.

[0041] In the clock regeneration circuit according to the embodiment of the invention described above, the direct digital synthesizer 6 is used by way of example. Instead of the direct digital synthesizer 6, other frequency dividers may also be used. Also, in the clock regeneration circuit according to the embodiment of the invention described above, although QPSK is used as a digital modulation method, other modulation methods such as PSK, ASK, QAM, FSK and MSK may also be used, with similar advantages being expected.

SECOND EMBODIMENT

[0042] A clock regeneration circuit according to another embodiment of the invention is shown in Fig. 4. Referring to Fig. 4, an AM data multiplex modulated signal is supplied to a frequency converter 201 to be converted into an intermediate frequency. The AM data multiplex modulated signal converted into the intermediate frequency is band-limited by a band-pass filter 202 having a narrower band than the band width of the AM data multiplex modulated signal. The band-pass filter 202 extracts the carrier of the AM modulated signal from the AM data multiplex modulated signal.

[0043] The carrier extracted by the band-pass filter 202 is further supplied to a limiter 203 in which AM modulated components which are not removed by the band-pass filter 202 are removed. An output of the limiter 203 is supplied to a phase comparator 204. An output of the phase comparator 204 is supplied to a loop filter 205 composed of a low-pass filter to smooth the output of the phase comparator which is supplied to a voltage-controlled oscillator 206 as a frequency

as a regenerated clock sign and also supplied to a direct d tal synthesizer 207.

[0044] The direct digital synthesizer 207 outputs waveform data having a frequency equal to the frequency-converted carrier frequency, for example, in accordance with an oscillation output of the voltage-controlled oscillator 206. The waveform data output from the direct digital synthesizer 207 is supplied to a D/A converter 208 to be converted into an analog signal. The frequency of the converted analog signal is equal to the frequency-converted carrier frequency, and after aliasing components of the analog signal are removed at a low-pass filter 209, the signal is supplied to the phase comparator 204. In accordance with an output from the phase comparator 204, the oscillation frequency of the voltage-controlled oscillator 206 is controlled.

[0045] An oscillation output from the voltage-controlled oscillator 206 is also supplied to another direct digital synthesizer 210 which outputs waveform data having a frequency equal to the local oscillation frequency. The waveform data output from the direct digital synthesizer 210 is supplied to a D/A converter 211 to be converted into an analog signal. The frequency of the converted analog signal is equal to the local oscillation frequency, and after aliasing components of the analog signal are removed at a low-pass filter 212, the signal is supplied to the frequency converter 201 as a local oscillation output to thereby convert the AM data multiplex modulated signal into an intermediate frequency.

[0046] In the clock regeneration circuit constructed as above according to the second embodiment of the invention, the AM data multiplex modulated signal is converted into the intermediate frequency, the band-pass filter 202 extracts the carrier of the AM modulated signal from the AM data multiplex modulated signal converted into the intermediate frequency, AM modulated components of the extracted carrier which are not removed by the band-pass filter 202 are removed by the limiter 203, and the carrier is supplied to the phase comparator 204 as a reference signal.

[0047] An output of the phase comparator 204 is smoothed by the loop filter 205, and the oscillation frequency of the voltage-controlled oscillator 206 is controlled in accordance with an output of the loop filter 205. An oscillation output of the voltage-controlled oscillator 205 is supplied to the direct digital synthesizer 207 which outputs the waveform data having a frequency equal to the frequency-converted carrier frequency. The waveform data is converted into an analog signal by the D/A converter 208, and after aliasing noises are removed by the low-pass filter 209, the phase of the analog signal is compared by the phase comparator 204 with the carrier of the frequency-converted AM modulated signal output from the limiter 203.

[0048] If the frequency of an output signal from the D/A converter 208 is different from the carrier frequency of the frequency-converted AM modulated signal, a beat corresponding to the frequency difference is superposed upon an output of the loop filter 205 so that the oscillation frequency of the voltage-controlled oscillator 206 is changed. Accordingly, the frequencies of the waveform data output from the direct digital synthesizers 207 and 210 are changed so that the frequencies of the output signals from the D/A converters 208 and 211 are changed. Therefore, the

the carrier frequency of the frequency-converted AM modulated signal, and then the output signal via the low-pass filter 212 from the D/A converter 211 converges to the local oscillation frequency used for frequency conversion. Accordingly, the oscillation frequency of the voltage-controlled oscillator 206 is synchronized with the carrier of the frequency-converted AM modulated signal.

[0049] An oscillation output from the voltage-controlled oscillator 106 therefore, becomes, a clock signal synchronized with the carrier of the AM modulated signal, and the oscillation output from the voltage-controlled oscillator 206 can be used as a clock signal for demodulating a digital modulated signal separated from the AM data multiplex modulated signal.

[0050] As described so far, according to the clock regeneration circuit of the invention, it is possible to regenerate a clock signal for data demodulation from an AM data multiplex modulated signal obtained by multiplexing a digital modulated signal and an AM modulated signal in the same frequency band and at the same time.